Linux *Kernel Hacking* Free Course 2003

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What I/O driver designers should know about the IBM-compatible PC architecture

The I/O bus

- A I/O bus consists of a set of wires:
  - Data wires, each of which can transfer one bit at a time
  - Address wires, which identify an I/O device
  - Control wires for power supply, verification signals, chip select, etc.
- Several I/O devices can be connected to the same bus
- Internal slots allow to connect add-on components

Evolution of the bus system

- 1980: a single bus connecting all I/O devices, including RAM to the CPU
- 1987: two buses, a system bus connecting the RAM to the CPU and an I/O bus
- Today: several I/O buses, system bus expanded to connect directly both RAM and graphic card to the CPU (AGP)

Three classic buses

- ISA: an old low speed bus, many cheap ISA expansion cards available, serial ports and parallel ports are on the ISA bus
- PCI: much faster than ISA, used to connect disk controllers and network cards
- USB: offers a standardized connector for attaching all the common I/O devices to a single port

Other buses

- SCSI: a sophisticated bus used in high performance systems
- FireWire (IEEE 1394): a high speed serial bus for storage and video
- USB 2.0: a 10-times faster USB-compatible enhancement

Some technical data

- ISA: 16 bit, syncronous with CPU, 8 MB/s
- PCI: 32 or 64 bits, asynchronous with CPU, 33MHz or 66 Mhz, upper limit of 528 MB/s
- USB: serial, 1.2 MB/s
- FireWire: serial, 80 Mb/s
- USB 2.0: serial, 12-40 MB/s

System buses

- 64-bit wide very fast buses connecting a device directly to the CPU
- Also called local buses, main buses, or processor buses
- They allow the CPU to access the RAM at full speed

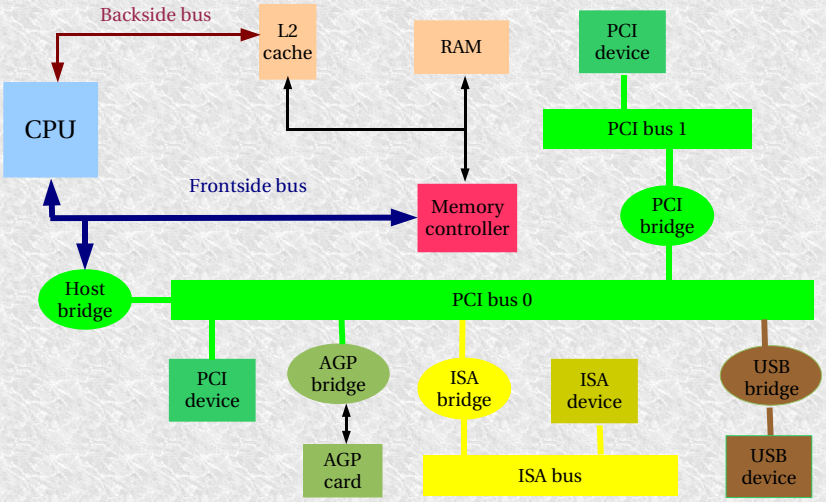
The AGP bus

- 3D graphics threatens to eat up all the available bandwith of a PCI bus
- The Accelerated Graphics Port is a system bus that allows fast transfers of data between the RAM and the graphic card
- The Direct Memory Execute (DIME) feature allows graphic cards to use RAM to compute things such as texture mapping and object hiding
- Screen images must still be sent to the frame buffer of the graphic card

Bus adapters

- The backbone bus of modern PCs is the PCI bus
- Compatibility with other buses such as ISA or USB is achieved by means of bus adapters, also called bus bridges

Typical bus layout



I/O ports on ISA bus

- Each device connected to the I/O bus has its own set of I/O addresses called I/O ports
- The I/O address space provides up to 65536 8-bit I/O ports
- Four special assembly language instructions called `in`, `ins`, `out`, and `outs` allow the CPU to read from and write to an I/O port
- The I/O ports of each device are structured into a set of specialized registers: control, status, input, and output

I/O ports on PCI bus

- The I/O address space accessed through `in` and `out` instructions includes up to 2^{32} 8-bit I/O ports
- I/O ports may be mapped into 32-bit or 64-bit memory addresses

I/O shared memory

- Several devices include their own memory called I/O shared memory
- The I/O shared memory can be accessed by means of the usual mov instructions by sacrificing part of the programmer's address space
- ISA bus: `0xe00000-0xffffff` are reserved addresses (the well known 640KB-1M hole)
- PCI bus: addresses close to the fourth GB are reserved for several PCI devices

I/O interfaces and controllers (1)

- I/O interfaces are circuits inserted between a group of I/O ports and the corresponding device controller
- The I/O interface translates the I/O port values into commands and data for the device. It also detects changes in the device state and updates the I/O port that plays the role of status register
- They can be connected through an IRQ line to a Programmable Interrupt Controller (see later)

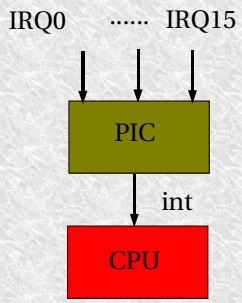
I/O interfaces and controllers (2)

- Complex devices require a device controller to drive it
- Such controller:
  - interprets the high-level commands received from the I/O interface
  - Converts and interprets the electrical signals received from the device and modifies, through the I/O interface, the value of the status register

Handling the requests for interrupt

- The I/O device signals an event that requires immediate attention
- The I/O interface of such device raises an IRQ signal that reaches the Programmable Interrupt Controller (PIC) chip
- The PIC polls continuously the IRQ lines connected to it; when it detects a signal on one of them, it raises the INT line connected to the CPU chip
- If interrupts are not disabled, the CPU switches control to handle the interrupt

The Programmable Interrupt Controller



Assigning IRQs to I/O devices

- The PCI bus system allows some flexibility
- Each I/O interface offers a range of port addresses and of IRQs
- The objective is to separate the I/O ports and to assign, if possible, a separate IRQ to each I/O device
- IRQ sharing is possible on the PCI bus
- Detecting which among several I/O device issued the IRQ is a task demanded to the kernel

The DMA controller (1)

- The DMAC is an auxiliary processor, which can be instructed by PCI devices to transfer data between the RAM and I/O devices
- Once activated by the CPU, the DMAC is able to continue the data transfer on its own
- The DMAC is mostly used by disk drivers and other slow devices that transfer a large number of bytes at once
- Its setup time is high, not appropriate for transfering small amount of data

The DMA controller (2)

- The DMAC is able to sustain several data transfers for different I/O devices
- When the DMAC terminates the transfer relative to an I/O device, it signals the I/O controller, which, in turn, signals the PIC via an IRQ

Hot pluggable devices

- A bus supports hot pluggable devices if these devices can be attached, configured, used, and detached while the system and other peripherals are in operation
- USB supports hot pluggable devices
- PCI supports hot pluggable devices
- All PCMCIA and CardBus devices are hot-pluggable